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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,569	10/16/2003	Beom-Jun Jin	SEC.872D	7173

7590 07/13/2004

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EXAMINER	
WILSON, SCOTT R	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,569	JIN ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-11 and 13-20* is/are rejected.

7)☒ Claim(s) *3,4,7 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Graettinger et al.. Graettinger et al., Figure 14, discloses a semiconductor memory device having a storage node contact hole (850) aligned at bit line spacers (Figure 2, element 130) formed at both side walls of a bit line stack (120) and exposing a pad (1100), the device comprising a multi-layered storage node contact plug (col. 5, line 64) formed in the storage node contact hole (850), the multi-layered storage node contact plug having a first storage node contact plug (1200) and a second storage node contact plug (610) formed on the first storage node contact plug.

As to claim 2, Graettinger et al. discloses (col. 7, lines 40-44) that the first storage node contact plug (1200) is formed of titanium nitride and the second storage node contact plug (610) is formed from polysilicon (col. 5, lines 32-33).

As to claim 5, Graettinger et al., Figure 14, discloses (col. 5, lines 54-55) a barrier metal layer (800) formed on the second storage node contact plug, wherein the barrier metal layer functions as a third storage node contact plug (col. 5, line 64).

As to claim 6, Graettinger et al. discloses (col. 5, line 55) that the barrier metal layer is formed from titanium nitride.

As to claim 8, Graettinger et al., Figure 14, discloses that the second storage node contact plug (610) is thicker than the first storage node contact plug (1200).

Claims 9-11 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Graettinger et al.. Graettinger et al., Figure 14, discloses a semiconductor memory device comprising a pad (1100)

formed on a semiconductor substrate, an interlayer dielectric layer (150) formed on the pad and substrate to insulate the pad, a bit line stack (120) formed on the interlayer dielectric layer, a pair of bit line spacers (130) formed at both side walls of the bit line stack, a storage node contact hole (850) formed within the interlayer dielectric layer, exposing the pad and aligned between the bit line spacers, and a multi-layered storage node contact plug formed within the storage node contact hole, including a first storage node contact plug (1200) and a second storage node contact plug (610) formed on the first storage node contact plug.

As to claim 10, Graettinger et al. discloses (col. 7, lines 40-44) that the first storage node contact plug (1200) is formed of titanium nitride and the second storage node contact plug (610) is formed from polysilicon (col. 5, lines 32-33).

As to claim 11, Graettinger et al. (col. 4, lines 1-4) discloses the bit line stack to be comprised of a bit line barrier metal layer (124), a bit line conductive layer (122) and a bit line cap layer (140), which are sequentially deposited.

As to claim 13, Graettinger et al., Figure 14, discloses a barrier metal layer (800) formed on the second storage node contact plug.

As to claims 14-20, the device of Graettinger et al. would necessarily have to be formed in order to function, so that the method comprising the means of forming the device is inherent in the device structure itself.

Allowable Subject Matter

Claims 3 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed multi-layer contact plug with an ohmic contact layer formed under the first contact plug.

Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed multi-layer contact plug formed over a polysilicon pad.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. No prior art discloses the claimed memory device with a bit line stack formed with a titanium nitride barrier metal layer, a conductive tungsten layer and a silicon nitride cap layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

srw
July 9, 2004